In the Claims:

Claim 1 (currently amended): A semiconductor workpiece, comprising:

a metal layer, wherein the metal layer has topical non-planarities extending from the metal layer;

an inorganic dielectric ARC layer disposed directly on the metal layer and directly on the topical non-planarities extending from the metal layer, wherein said inorganic dielectric ARC layer functions as a hard mask, and wherein said inorganic dielectric ARC layer has a substantially uniform thickness over the topical non-planarities extending from the metal layer; and

a photoresist layer disposed on the ARC layer opposite the metal layer.

Claim 2 (original): The workpiece recited in claim 1 wherein the ARC layer comprises silicon oxynitride.

Claim 3 (original): The workpiece recited in claim 2 wherein the ARC layer consists essentially of silicon oxynitride.

Claim 4 (canceled).

Claim 5 (currently amended): The workpiece recited in claim [4]1 wherein the ARC layer is deposited on the metal layer by chemical vapor deposition.

Claim 6 (original): The workpiece recited in claim 5, wherein the ARC layer is deposited on the metal layer by plasma enhanced chemical vapor deposition.

Claim 7 (original): The workpiece recited in claim 1 wherein the photoresist layer is between 0.1 to 2 microns thick.

Claim 8 (currently amended): The workpiece recited in claim 7 ~~where in~~wherein the photoresist layer is 0.6 to 1.0 microns thick.

Claim 9 (currently amended): A metallic stack for a semiconductor interconnect, comprising:

a metal layer, wherein the metal layer has topical non-planarities extending from the metal layer;

an inorganic dielectric ARC layer disposed directly on the metal layer and directly on the topical non-planarities extending from the metal layer, wherein said inorganic dielectric ARC layer functions as a hard mask, and wherein said inorganic dielectric ARC layer has a substantially uniform thickness over the topical non-planarities extending from the metal layer; and

a barrier layer disposed on the metal layer opposite the ARC layer.

Claim 10 (original): The metallic stack recited in claim 9 wherein the ARC layer comprises silicon oxynitride.

Claim 11 (original): The metallic stack recited in claim 10 wherein the ARC layer consists essentially of silicon oxynitride.

Claim 12 (canceled).

Claim 13 (currently amended): The metallic stack recited in claim ~~12~~9 wherein the ARC layer is deposited on the metal layer by chemical vapor deposition.

Claim 14 (original): The metallic stack recited in claim 13 wherein the ARC layer is deposited on the metal layer by plasma enhanced chemical vapor deposition.

Claim 15 (previously presented): The metallic stack recited in claim 9 wherein the stack is about 1,000 to 20,000 Angstroms thick.

Claim 16 (previously presented): The metallic stack recited in claim 15 wherein the stack is about 5,000 to 8,000 Angstroms thick.

Claim 17 (previously presented): A semiconductor device, comprising:

an oxide layer formed on a wafer; and

at least one microelectronic structure extending from the oxide layer and including:

a barrier layer disposed on the oxide layer;

a metal layer disposed on the barrier layer;

an inorganic dielectric ARC layer disposed directly on the metal layer, wherein said inorganic dielectric ARC layer functions as a hard mask; and

a residual photoresist layer disposed directly on said inorganic dielectric ARC layer.

Claim 18 (canceled).

Claim 19 (original): The semiconductor device recited in claim 17 wherein the ARC layer consists essentially of silicon oxynitride.

Claim 20 (original): The semiconductor device recited in claim 19 wherein the ARC layer is formed by plasma enhanced chemical vapor deposition.